REMARKS

The present invention is directed to a light source and a light emitting diode capable of providing a relatively low powered light with a high production rate and a semiconductor light emitting device that can be tested for optical performance characteristics such as any unevenness of color before being mounted in a finished lamp assembly. These design goals are accomplished without increasing the size of the semiconductor light emitting device. The semiconductor light emitting diode can be formed in an array as a chip, for example with the individual LEDs connected in series. Appropriate power supply terminals and through holes within the semiconductor substrate can be utilized in a manner such that the power supply terminals will have appropriate heat dissipation to improve the light emitting characteristics.

Additionally, a phosphor film can have a characteristic of converting the wavelength of light emitted from a light emitting layer in the LED, so basically a combination of blue light and yellow light can be mixed together to generate an output of white light. The phosphor layer can cover not only the upper structure of the LED, but the side surfaces too, to ensure that any blue light emitted from a side surface is also subject to an appropriate conversion. The LED arrays can be mounted, for example in a light emitting structure as shown in Figure 8.

As can be appreciated, the conservation of power has created a new impetus for economical and efficient lighting devices and a large number of scientists and engineers from major international companies have attempted to address this issue.

> "Thus when differences that may appear technologically minor nonetheless have a practical impact, particularly in a crowded field, the decision-maker must consider the obviousness of the new structure in this light."

> *Continental Can Co. USA Inc. v. Monsanto Co.*, 20 U.S.P.Q. 2d. 1746, 1752 (Fed. Cir. 1991).

Newly drafted Claim 35 incorporates features such as set forth previously in dependent Claim 5.

The Office Action contended that Claims 1-3, 5-6, 11 and 34 were contended to be completely anticipated by *Ohtuka et al.* (WIPO Patent Application Publication No. WO/058726) under 35 U.S.C. §102.

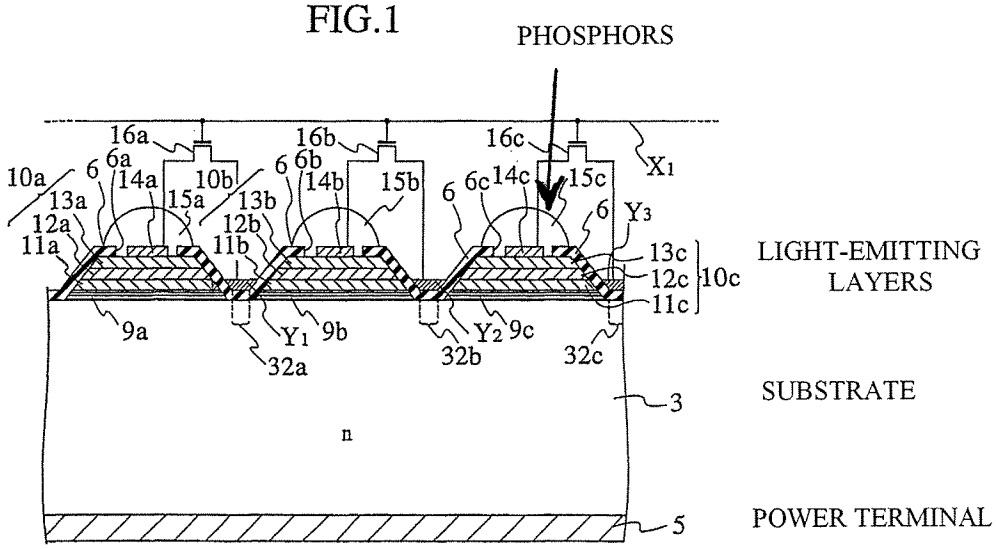
> "'[T]he dispositive question regarding anticipation is whether one skilled in the art would reasonably understand or infer from the prior art reference's teaching that every claim [limitation] was disclosed in that single reference.' *Dayco Prods., Inc. v. Total Containment, Inc.*, F.3d 1358, 1368 (Fed. Cir. 2003).

New independent Claim 35 sets forth a semiconductor light emitting device of a particular configuration of a multilayer epitaxial structure with power supply terminals and connections through holes in the base substrate so that appropriate first electrodes and second electrodes can be connected to conductive layers that sandwich a light emitting layer. Thus, heat dissipation is achieved while providing a structure to facilitate an efficient manufacturing procedure.

Phosphor film covers not only the main surface of the multilayer epitaxial structure, but also side surfaces so that an even color of white can be achieved even if the light emitting layer emits near ultraviolet light.

The *Ohtuka et al.* reference discloses a semiconductor light emitting device as shown in Figure 1 of three separate light emitting device layers, respectively 10a, 10b and 10c as shown on a substrate 3 in the following illustration:

FIG.1



As can be readily determined the *Ohtuka et al.* reference does not teach the following claim features such as for a first and second power supply terminals formed on the main surface of the base substrate, which faces away from a multilayer epitaxial structure. A first conductive member which includes a first through hole that is provided in the base substrate and electrically connects the first electrode and the first power supply terminal, a second conductive member, which includes a second through hole that is provided in the base substrate and electrically connects the second electrode and the second power supply terminal, and phosphor that not only covers a main surface of the multilayer epitaxial structure, but further includes every side surface of the multilayer epitaxial structure from a layer including the main surface to at least the light emitting layer.

The *Ohtuka et al.* reference discloses, for example in the above Figure 1, only one power supply terminal 5 formed on a main surface of the base substrate which faces away from the multilayer epitaxial structure 10a-10c.

Additionally, the *Ohtuka et al.* reference does not disclose a structure including a through hole included in a base substrate 3 to connect the first electrode Y1 with a second electrode 14a and the power supply terminal 5.

The phosphor 15a, 15b and 15c is a hemispherical configuration extending over the second electrodes and only a portion of the exposed light emitting layer 13c.

Ohtuka et al. actually teaches a substrate 3 supporting a Bragg reflector 9a, 9b, 9c with light-emitting layers 11, 12, 13 deposited over the Bragg reflector. The substrate 3, Bragg reflector and light emitting layers are then coated with a silicon oxide film 6 with a narrow window 6a. See US Patent Publication No. 2006/0175621 of the *Ohtuka et al.* co-pending application at Paragraph [0030].

The Office Action asserted that through holes 32a-32c were provided in the substrate. Applicant respectfully traverses this assertion since 32a-32c are actually elongated grooves, seen also in Figure 2 that crosses the elongated grooves 31a-31c. The first elongated grooves 32a-32c carry source electrodes Y_1, Y_2, Y_3 and the second elongated grooves 31a-31c carry gate electrodes X_1, X_2, X_3, see Paragraph [0031]. Interlayer insulating films 17a to 17i are also used along with the silicon oxide film.

As can be appreciated, the phosphors 15a-15c is only over the windows and the silicon oxide film 6 covers the sides of the light emitting layers.

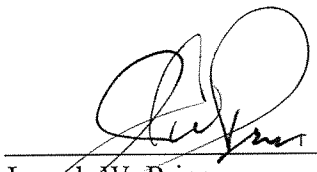
The other reference's cited record, for example *Lowery* (European Patent Application 1198016) basically is cited for disclosing a method of forming a luminescence layer with the use of a stencil. The other references were cited for secondary features to be combined with the *Ohtuka et al.* reference.

It is believed that the above comments distinguishing the teaching of the *Ohtuka et al.* reference as a basic reference, either under 35 U.S.C. §102 or in a combination with the secondary references under 35 U.S.C. §103. None of the references teach the features in the current independent Claim 35 and accordingly, Claim 35 and the dependent Claims 36-45 should be allowable.

If the Examiner has any questions with regards to the prosecution of this case, the undersigned attorney can be contacted at the listed phone number.

Very truly yours,

SNELL & WILMER L.L.P.



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